AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 7 (Canceled)

Claim 8 (Original): A method of manufacturing a semiconductor device, comprising the steps of:

forming two layers of a gate insulating film and a gate electrode on a partial area of a surface of a semiconductor substrate;

forming a lamination film on surfaces of the semiconductor substrate, gate insulating film and gate electrode conformable to the surfaces, the lamination film having a structure of at least three layers, each of the three layers being made of insulating material, and a middle layer being made of material easier to trap carriers than other two layers;

forming a conductive side wall spacer on a surface of the lamination film in areas along a side wall of the gate electrode;

etching the lamination film at least to a bottom of the middle layer in an area not covered with the side wall spacers;

implanting first impurities into a surface layer of the semiconductor substrate by using the

gate electrode and the side wall spacer as a mask;

forming a first insulating film by locally oxidizing the surface of the semiconductor substrate not covered with the gate electrode and the side wall spacer;

removing an insulating film formed on an upper surface of the gate electrode and on a surface of the side wall spacer; and

forming a connection member electrically connecting the upper surface of the gate electrode and the surface of the side wall spacer.

Claim 9 (Original): A method according to claim 8, wherein:

a two-layer structure of the gate insulating film and gate electrode extends in a first direction on the surface of the semiconductor substrate and is formed in each of a plurality of areas disposed in parallel to each other; and

said step of forming the connection member comprises:

a step of covering a whole surface of the semiconductor substrate with a conductive film;

a step of patterning the conductive film to leave a plurality of gate lines extending in a second direction crossing the first direction and disposed in parallel to each other;

a step of etching the gate electrode by using the gate lines as a mask after the gate lines are left; and

a step of implanting second impurities of a conductivity type opposite to the first impurities into a surface layer of the semiconductor substrate under an area where the gate electrode was etched.

Claim 10 (Original): A method of manufacturing a semiconductor device, comprising the steps of:

forming three layers of a gate insulating film, a gate electrode and a gate upper film on a partial area of a surface of a semiconductor substrate;

forming a lamination film of a lower layer, a middle layer and an upper layer, the lower layer covering exposed surfaces of at least the semiconductor substrate, gate insulating film and gate electrode, the middle layer covering surfaces of the lower layer and gate upper film, the upper layer covering the middle layer, each of the lower, middle and upper layers being made of insulating material, and the middle layer being made of material easier to trap carriers than the lower and upper layers;

forming a first conductive film covering a surface of the lamination film;

anisotropically etching the lamination film and first film to leave a side wall spacer, which is made of a portion of the first film, and a portion of the lamination film on a side wall of the gate electrode and gate upper film, and to remove at least the first film and the upper and middle layers of the lamination film on the surface of the semiconductor substrate in an area where the gate electrode is not disposed;

implanting first impurities into a surface layer of the semiconductor substrate by using the gate electrode, gate upper film and side wall spacer as a mask;

forming a second film of insulating material on or over a whole surface of the semiconductor substrate;

polishing the second film until the gate upper film is exposed;

removing the gate upper film and the lamination film left on the side wall of the gate upper film; and

forming a connection member electrically connecting an upper surface of the gate electrode and an exposed surface of the side wall spacer.

Claim 11 (Original): A method according to claim 10, wherein:

a three-layer structure of the gate insulating film, gate electrode and gate upper film extends in a first direction on the surface of the semiconductor substrate and is formed on each of a plurality of areas disposed in parallel to each other; and

said step of forming the connection member comprises:

a step of covering a whole surface of the semiconductor substrate with a third conductive film;

a step of patterning the third film to leave a plurality of gate lines extending in a second direction crossing the first direction and disposed in parallel to each other;

a step of etching the gate electrode, at least an upper layer of the second film and the side wall spacer by using the gate lines as a mask after the gate lines are left; and

a step of implanting second impurities of a conductivity type opposite to the first impurities into a surface layer of the semiconductor substrate under an area where the gate electrode was etched.

Claims 12 –13 (Canceled)

Claim 14 (Withdrawn): A method of manufacturing a semiconductor device comprising the steps of:

sequentially forming a gate insulating film, a carrier trap film made of material easier to trap carriers than the gate insulating film, and an upper insulating film on a surface of a semiconductor substrate;

forming resist patterns on or over the surface of the semiconductor substrate, the resist patterns covering surfaces of the upper insulating films formed in a pair of elongated first channel regions disposed in parallel to each other and spaced apart by some distance;

etching the upper insulating film and carrier trap film by using the resist patterns as a mask;

implanting impurity ions into a surface layer of the semiconductor substrate under conditions that an area between the pair of resist patterns is shaded by one of the resist patterns so that impurity ions are not implanted into the shaded area, and that in each of areas outside of the pair of resist patterns, boundaries of the ion implanted areas become coincident with boundaries of the resist patterns or extends from the boundaries of the resist pattern to an inside region;

removing the resist patterns;

forming a first film made of insulating material on the surface layer of the semiconductor substrate in the area implanted with ions by said impurity ion implanting step; and

forming a gate electrode on the upper insulating films covering the carrier trap films over the pair of first channel regions and on the gate insulating film between the pair of first channel regions.

Claims 15 - 18 (Canceled)

Claim 19 (Withdrawn): A method of manufacturing a semiconductor device comprising the steps of:

sequentially forming a gate insulating film, a carrier trap film made of material easier to trap carriers than the gate insulating film, and an upper insulating film on a surface of a semiconductor substrate;

forming resist patterns on the upper insulating film, the resist patterns covering a pair of elongated areas disposed in parallel to each other and spaced apart from each other by some distance;

etching the upper insulating film and carrier trap film by using the resist patterns as a mask;

implanting impurity ions into a surface layer of the semiconductor substrate by using the resist patterns as a mask;

removing the resist patterns;

forming a first film made of insulating material in the surface layer of the semiconductor substrate in the area implanted with ions by said impurity ion implanting step; and

forming a gate electrode on the upper insulating films and the first film between the upper insulating films.

Claim 20 (Withdrawn): A method according to claim 19, wherein the semiconductor substrate is a silicon substrate, and in said first film forming step, the first film is formed by locally oxidizing a surface layer of the semiconductor substrate by using the carrier trap films as a mask.

Claim 21 (Withdrawn): A method of manufacturing a semiconductor device comprising the steps of:

covering a pair of elongated areas disposed in parallel to each other and spaced apart from each other by some distance on a surface of a semiconductor substrate made of silicon, with resist patterns;

implanting impurity ions into a surface layer of the semiconductor substrate by using the resist patterns as a mask;

oxidizing the surface layer of the semiconductor substrate to form a first film of silicon oxide on a surface of an area where impurity ions were implanted and to form gate insulating films thinner than the first film on a surface of an area where impurity ions are not implanted;

sequentially forming a carrier trap film made of material easier to trap carriers than the gate insulating film and an upper insulating film on the first film and gate insulating film; and

forming a gate electrode on a surface of the upper insulating film in an area on or over at least the gate insulating films and the first film between the gate insulating films.